REMARKS

Applicants find no rejection of claims 31 and 32, which were added in Applicants response filed on October, 11, 2005. Applicants believe that the limitations of claims 31 and 32 are clearly patentable over Osann et al. as discussed *infra*. Applicants respectfully request the Examiner provide an Examination of claims 31 and 32.

The Examiner rejected claims 1-30 under 35 U.S.C. §102(b) as allegedly being anticipated by Osann et al., JR. *et al.* (Osann et al.) (US 2002/0010903).

Applicants respectfully traverse the §102 rejections with the following arguments.

35 U.S.C. §102

Applicants believe that a major difference between Ossan et al. and Applicants invention, is that in Ossan et al. teaches a increasing the size of a PLA design and changing the function of the PLA in hardware, while Applicants teach changing the function of the design of the PLA.

As to claims 1 and 16, Applicants respectfully contend that Osann et al. does not anticipate claims 1 and 16, because Osann et al. does not teach each and every feature of claims 1 and 16.

In a first example, Osann et al. does not teach "modifying a high-level design of said state machine to obtain a modified high-level design of said state machine with a modified function."

The Examiner states "Osann et al. discloses ....a) modifying a high-level design of said state machine (logic block) to obtain a modified high-level design of said state machine with a modified function (pg. 3, ¶ 39, ll. 5-14). In the Examiner's response to arguments, the Examiner stated "modification of the functionality in the event of later reprogramming will be required for the particular reconfigurable block, such as a state machine, and the software that the specified description of the designated functionality to model PLA, This modeled PLA structure (with added capacity) is then incorporated into the rest of the ASIC design. The ASIC device is functionality defined HDL or other functionally similar language."

Applicants respectfully point out that, in FIG. 9 a PLA format file (1106) is converted by PLA structural netlist generator (1110) in to structural netlist for PLA (1112) having additional capacity not a modified function. Osann et al. page 3, paragraph 43 teaches "additional capacity 1108 is added to PLA format file 1106 to accommodate changes and/or modifications in functionality **later**) in step 1110 to generate structural netlist for 1112 for the PLA." Note that

Osann et al. clearly differentiates between capacity and functionality. Further, Osann et al. teaches on page 3, paragraph 39 "to allow for expansion or modification of the functionality in the event of later reprogramming." It is clear that netlist 1112 does not have a modified function. Still further, Ossan et al. teaches on page 4, paragraph 52 that "a revised programming file 1142 is generated that contains the programming pattern that is to be loaded into the already **built** ASIC 1126." Since this reprogramming is performed on hardware not on the design Ossan et al. is not teaching "a modified high-level **design** of said state machine with a modified function" as Applicants claims 1 and 16 require.

In a second example, Osann et al. does not teach "generating a programmable logic device netlist from differences in said high-level design and said modified high-level design."

The Examiner states Ossan et al. discloses "b) generating a programmable logic device netlist from differences in said high-level design and said modified design (pg. 3, ¶ 43 and ¶ 48, ll. 1-9; ¶ 52, ll. 3-9)." In the Examiner's response to arguments, the Examiner stated " additional capacity is add to PLA format file (to accommodate changes and/or modification in functionality later) to generate netlist for PLA, which is from the difference the high-level design and the modified high-level design." and "the additional capacity (the difference between the 'high-level design' and the 'modified high level design) can be determined either circuit designer or automatically by software."

Applicants respectfully point out that Osann et al. page. 3, ¶ 43 and ¶ 48, ll. 1-9 are part of the section "Creating a PLA Within an ASIC" and Osann et al page 4, ¶ 52, ll. 3-9 are part of the section "Generating a Programming Pattern" and the Examiner appears to have combined two

different and distinct operations. Applicants respectfully point out (1) Osann et al. (pg. 3, ¶ 43) teaches "The amount of additional capacity 1108 can be determined by the circuit designer or it can be added automatically by software" is simply a statement of how to determine how much additional capacity to add; (2) Osann et al. (pg. 3, ¶ 48, ll. 1-9) teaches "once structural netlist for PLA 1112 and the netlist for the rest of the ASIC 1118 are generated, then functional simulations can be run" does not include doing anything with "differences"; and (3) Osann et al. (pg. 4; ¶ 52, ll. 3-9) is a description of FIG. 10, which is operating only on "the new PLA functionality 1102' " and is a stand alone operation on PLA format file 1106' and does not compare 1106' with anything else.

In a third example, Osann et al. does not teach "installing said modified function into said state machine by programming said programmable logic device based on said programmable logic device netlist." The Examiner stated Ossan et al. discloses "(c) installing (loading) said modified function into said state machine by programming said programmable logic device based on said programmable logic device netlist (pg. 4, ¶ 52, ll 3-13)."

Applicants respectfully point out that, in FIG. 10 and the corresponding description of FIG. 10 on page 4, paragraph 52. Osann et al. is teaching converting (step 1104) a high-level design of a state machine (1102') into programmable logic device format file (1106'), which is an operation performed a modified file 1106' not the unmodified file 1106 of FIG. 9 and that modified file 1106' is complete description of the PLA and therefore Osannet al is not "installing said modified function into said state machine by programming said programmable logic device based on said programmable logic device netlist" as Applicants claim 1 and 16 require.

In the Examiner's response to arguments, the Examiner stated in part " Osann et al. does not always teach processing the difference between two HDL files ... page 3 ¶ 43 ... Furthermore, pg. 4, ¶ 52, the HDL description of the new (modified) PLA functionality mapping in the previous structure netlist for revised the programming. Therefore Osann et al. does not always teach processing the difference between two HDL files ..."

Applicants fail to understand the Examiners response, as Applicants have maintained that Osann et al. never teaches processing the differences between two HDL files.

Based on the preceding arguments, Applicants respectfully maintain that Osann et al. does not anticipate claims 1 and 16, and that claims 1 and 16 are in condition for allowance. Since claims 2-15 and 31 depend from claim 1 and claims 17-30 and 32 depend from claim 16, Applicants contend that claims 2-15,17-32 are likewise in condition for allowance.

As to claims 3 and 18, Applicants contend that Ossan et al. does not teach "said extracting includes comparing said high-level design to said modified high-level design." The Examiner stated Osann et al. discloses "wherein said extracting includes comparing (simulation) said high-level design to said modified high-level design (Pg. 3, ¶ 44, ll 4-15; ¶ 47; and ¶ 48, 11. 5-15)." Applicants respectfully point out that Ossan et al. (Pg. 3, ¶ 44, ll. 4-15) is not teaching simulation or comparing; Osann et al. (Pg. 3, col 47) is not teaching simulation or comparing, and Ossan et al. (Pg. 3, ¶ 48, ll. 5-15)is teaching simulation (1128) of first a netlist from (1112) and then of second (1118) (see also Osann et al. FIG. 9) and does not teach not comparing of the two netlists.

As to claims 11 and 26, Applicants contend that Ossan et al. does not teach "wherein said programmable logic device is connectable between a next stage logic and a state latch of said state machine in either a next state path, a current state path or both" as the Examiner alleges. Applicants point out that FIGs 13, 13a, 14 and 14A and page 5, paragraphs 74-76 are teaching core cell designs of a mask programmable array and not "state machines."

As to claims 14 and 29, Applicants find no teaching in Ossan et al. of "said programmable logic device is shared between said state machine and one or more additional state machines." Applicants point out that Ossan et al. FIG. 3 and page 1, paragraph 9 teaches the PLA has "AND" and "OR" sections. "AND" and "OR" sections are not "state machines." Applicants further point out that Ossan et al. FIG. 8 and page 3, paragraphs 40 and 43 teaches that there can be multiple PLAs. Ossan et al. does not teach multiple state machines and does not teach sharing a PLA between multiple state machines.

As to claims 31 and 32, Applicants point out that the because of the "HDL to PLA **conversion** (1104)" of Ossan et al., Ossan et al. is not teaching "said high-level design of said state machine and said high level-design of said state machine with said modified function are in the same file format" as Applicants claims 31 and 32 require.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

Respectfully submitted,
FOR: Goodnow et al.

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